"RESPONSE UNDER 37 CFR 1.116-EXPEDITED PROCEDURE EXAMINING

Docket No.

210067US2

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Hidemasa ZAMA, et al.

GAU:

2819

SERIAL NO: 09/883,959

EXAMINER: TAN, V.

FILED:

June 20, 2001

FOR:

SEMICONDUCTOR INTEGRATED CIRCUIT, LOGIC OPERATION CIRCUIT, AND FLIP FLOP

## REQUEST FOR EXTENSION OF TIME **UNDER 37 C.F.R. 1.136**

ASSISTANT COMMISSIONER FOR PATENTS WASHINGTON, D.C. 20231	TECHNOLOGY
SIR:	90JB VBV 公子C
It is hereby requested that a one month extension of time be granted to November 1, 2002 for	
■ filing a response to the Official Action dated: July 1, 2002	JVED 1 2002 CENTER
responding to the requirements in the Notice of Allowability dated:	83
☐ filing the Formal Drawings. The Issue Fee due has been timely filed.	00
responding to the Notice to File Missing Parts of Application dated:	
☐ filing a Notice of Appeal. A timely response to the final rejection, due	has been filed.
☐ filing an Appeal Brief. A Notice of Appeal was filed on:	
☐ Applicant claims small entity status. See 37 CFR 1\27. Therefore, the fee amount shown below	is reduced by one-half
The required fee of \$110.00 is enclosed herewith by check and any further charges may be made aga Record's Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.	ainst the Attorney of

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C.

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